Remarks

Four of the Japanese patent documents submitted on the Information Disclosure Statement filed October 17, 2005 were not considered by the Examiner. The Examiner stated that a legible copy of these four foreign patent documents could not be found in the file on record. Copies of these foreign patent documents were not submitted as they were identified in the International Search Report (ISR) for the underlying PCT application and copies of these foreign patent documents should have been received by the United States Patent and Trademark Office. Thus, at the time of filing of the Information Disclosure Statement, submission of the foreign patent documents was not required. However, for the Examiner's convenience, these foreign patent documents are provided herein and a clean copy of original form PTO/SB/08a for initially by the Examiner.

The specification is being amended at pages 16 and 17 to state that the solder resist layer is formed in a region of not less than ~~30%~~ 20% of the wiring patterns. Support for this amendment is provided in original claims 9 and 16.

Claims 2, 10, 12 and 14-16 are pending. Claims 1, 3-9, 11 and 13 have been cancelled. Claim 2 is the sole remaining independent claim.

Claim 2 has been amended to recite that an area occupied by one film carrier is substantially the same as an area of an electronic part to be mounted on the film carrier tape. Support for this amendment can be found in dependent claim 13. Accordingly, claim 13 has been cancelled. Claim 2 has also been amended to recite that in each film carrier, a distance between one section and its adjacent section of the divided solder resist layer is in the range of 20 μm to 3 mm. Support for this amendment can be found in the originally filed specification at page 17, lines 15-19. Claim 11 has been cancelled as it recites a broader range of 20 μm to 50 mm.

The abstract has been amended to remove the legal term "comprising" therefrom.

No new matter has been added.

Claims 1-6, 8-13 and 15-16 are rejected under 35 U.S.C §102(b) as being anticipated by Japanese Patent No. JP404365343 to Masahiko Saeki (hereinafter referred to as "Masahiko"). Claims 1, 3-9, 11 and 13 have been cancelled. Thus, the rejection of the remaining claims 2, 10, 12 and 15-16 over the teachings of Masahiko will be addressed below.

The Examiner alleges that Masahiko teaches each and every feature of the claims including a film carrier tape comprising an elongated insulating film having a plurality of metal wiring patterns formed thereon wherein the wiring patterns are each independently covered with a solder resist layer, except a connecting terminal portion, and the solder resist layer is divided into plural sections. According to the Examiner, Masahiko also teaches this division of the solder resist layer into sections to reduce the warp of the taper carrier as a result of heating. With respect to claim 2, the Examiner states that Masahiko in figure 1 discloses film carrier tape for mounting an electronic part wherein at least two of the wiring patterns are arranged side by side in the width direction of the elongated insulating film.

Applicant respectfully traverses the Examiner's rejection for the following reasons. Masahiko discloses a tape carrier for TAB (Tape Automated Bonding) tape that is produced by forming a wiring pattern on an insulating film and coating a thermosetting resin on the wiring pattern in a divided area to reduce the deformation of the TAB tape.

Contrary to the teachings of Masahiko, the present invention reduces warpage distortion of film carrier tapes for mounting electronic parts, which have film carriers each having substantially the same size as that of an electronic part to be mounted such as CSP (chip size package), BGA (ball grid array) and COF (chip on film), in which two or more film carriers are arranged on a tape of an elongated insulation film side by side in the width direction of the tape as described at page 1, lines 8-16 of the specification.

Masahiko fails to disclose the claimed feature of "at least two of said wiring patterns being arranged side by side in the width direction of the elongated insulating film" due to the difference of the film carriers to be used, as described above. It is noted that the Examiner asserts that figure 1 in Masahiko discloses that the wiring patterns are made of a conductive metal (copper) and at least two of the wiring patterns are arranged side by side in the width direction of the elongated insulating film. Applicant traverses the Examiner's position as Masahiko fails to disclose "an area occupied by one film carrier is substantially the same as an area of an electronic part to be mounted on the film carrier tape". Independent claim 2 has now been amended to recite this feature.

With respect to original claim 11, the Examiner asserts that "Masahiko further discloses a distance between one section and its adjacent section of the divided solder resist layer

is in the range of 20 μm to 50 mm (as the width of the film is 35 μm, the distance between the adjacent section is less than 35 mm, column 2, line 7, as translated by the translator)." Applicant respectfully traverses this statement as Masahiko is silent with respect to a distance between one section and its adjacent section of the divided solder resist layer being in the range of 20 μm to 3 mm in each film carrier. As stated in the specification at page 17, lines 20-22, when the distance between the sections is determined according to the disclosed range, the internal stress produced in one section is not transmitted to the adjacent section and the wiring pattern in each section is protected. Independent claim 2 has also been amended to recite that the distance between one section and its adjacent section of the divided solder resist layer is in the range of 20 μm to 3 mm in each film carrier.

For the reasons set forth above, it is respectfully requested that the rejection of claims 2, 10, 12 and 15-16 under 35 U.S.C. §102(b) be withdrawn as Masahiko fails to teach each and every limitation of the amended claims.

Claims 7 and 14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Masahiko in view of United States Patent No. 7,211,735 to Kaneda (hereinafter referred to as "Kaneda"). Claim 7 has been cancelled. The rejection of remaining claim 14 is addressed below. Kaneda is relied upon by the Examiner as teaching that forming metal balls/bumps is old and known in the art. The Examiner then alleges that it would have been obvious to provide the film carrier of Masahiko with the opposite surface being designed so that metal balls are arranged to enable electrical connection outside the film carrier. Applicant respectfully traverses this rejection for the following reasons.

Kaneda discloses a stock sheet for a multilayer flexible wiring board comprising a long flexible sheet-like substrate and a plurality of wiring patterns formed on a same surface of the substrate, each wiring pattern having connecting electrodes through the substrate and exposed on both sides of the substrate.

The present invention is directed to film carrier tapes for mounting electronic parts having film carriers such as CSP, BGA and COF, not TAB. As stated at page 3, line 5-page 4, line 4 of the present specification, "In a recent technique for mounting electronic parts, film carriers each having an area substantially the same as that of an electronic part to be mounted, such as COF (chip on film), CSP (chip size package) and BGA (ball grid array), have

been used more frequently. Because such a film carrier occupies a small area, plural film carriers (e.g., 2 or 4 film carriers) can be arranged side by side in the width direction of a tape made of an insulating film in the production of a film carrier tape. In CSP, COF, BGA or the like, a solder resist layer is formed in each of the film carriers, so that each film carrier having a solder resist layer suffers warpage, and even if reverse warpage is applied to the tape having plural film carriers formed side by side in the width direction, the tape is bent at the boundary between the film carriers adjacent to each other in the width direction. Therefore, effective reverse warpage cannot be given to each of the curved (warped) film carriers. Under the existing circumstances, accordingly, there is no effective warpage-removal method to correct warpage distortion of each film carrier in a film carrier tape for mounting electronic parts wherein plural film carriers are formed in the width direction of the tape such as CSP and BGA".

Thus, the object of the present invention, as stated at page 4, lines 9-13 of the specification, is to provide a film carrier tape for mounting electronic parts in which plural film carriers are formed in the width direction of the tape and warpage distortion of each film carrier is reduced.

Accordingly, the present invention has been accomplished for the first time by adopting a film carrier tape as defined in claim 2 and by constituting unexpected results as exemplified in the working examples of the specification. Furthermore, one having ordinary skill in the art would not be motivated to combine the teachings of Masahiko with Kaneda to arrive at the present invention as the goals of the references and the present invention are completely opposed with one another.

For the reasons set forth above, it is respectfully requested that the rejection of claim 14 under 35 U.S.C. §103(a) be withdrawn as the combination of Masahiko with Kaneda fails to render this claim obvious.

In view of the arguments and amendments to independent claim 2, it is respectfully requested that all claims remaining in the application, namely claims 2, 10, 12 and 14-16, be allowed and the application be passed to issue.

Respectfully submitted,

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